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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,542	03/23/2004	Yusuke Ota	9319S-000700	3775

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EXAMINER	
NADKARNI, SARVESH J	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,542	OTA, YUSUKE	
	Examiner	Art Unit	
	Sarvesh J. Nadkarni	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/14/2006 and 3/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed March 23, 2004, Application Number: 10/807,542 (hereinafter referred to as "application"). The application was published on December 2, 2004, Publication Number: 2004/0239606 A1. Receipt is acknowledged of the information disclosure statement, form PTO-892, filed on March 23, 2004 and March 14, 2006. Page and line number references made in this action relate to the originally filed application, not the publication.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. 37 CFR 41.154(b) and 41.202(e).

Failure to provide a certified translation may result in no benefit being accorded for the non-English application.

Claim Objections

3. **Claim 2** is objected to because of the following informalities: the element "shift output" within the wherein clause is not introduced using proper antecedent basis format; the article "a" or "an" is used to introduce an element, whereas "the" or "said" is used to refer to a previously introduced element or step. "Shift output" was properly introduced in **claim 2**, in the first line of

the claim. However, the subsequent reference to the element is improper. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., United States Patent Application Publication, Pub. No. US 2001/0011988 A1; Pub. Date: Aug. 9, 2001; (hereinafter referred to as "Ikeda") and further in view of Priem et al., United States Patent, Pat. Number: 5,805,133; Date of Patent: Sep. 8, 1998 (hereinafter referred to as "Priem '133").

5. With regard to **claim 1**, Ikeda clearly teaches

a display driver (see paragraph [0028] "liquid crystal driver") **for driving data lines** (see paragraph [0028] "plurality of data lines") **of an electro optic device** (see paragraph [0028] "liquid crystal display") **based on display data** (see paragraph [0028] "display data"), **comprising:**

a display data random access memory (see paragraph [0028] "memory" further described in detail as "SRAM" and "DRAM" in paragraph [196]) **including**

a plurality of word lines (see page 7, paragraph [194], describing the word line decoder (DEC) selecting a "word line" of many word lines of the memory)

a plurality of column lines (see page 7, paragraph [196], describing an of a "column address decoder (DEC)" selecting a signal line of the memory) **and**

a plurality of memory cells each storing display data of one pixel (see page 3, paragraph [0026] describing the display memory used for storing display data corresponding to the pixels and an address of the display data on the display screen designated into a corresponding address of the display memory; see additionally, FIG. 15 describing a memory map)

a display address decoder selecting a word line of the display data random access memory based on a display address; (see page 7, paragraph [194], describing the word line decoder (DEC) selecting a "word line" of many word lines of the memory

a display column address decoder selecting a column line of the display data random access memory based on a display column address; (see page 7, paragraph [196], describing a "column address decoder (DEC)" selecting a signal line of the memory)

6. However, **Ikeda** fails to teach a plurality of read-out bit lines each commonly coupled to a memory cell group specified by a corresponding column line; a scroll bus coupled to the plurality of read-out bit lines; a plurality of data latches each corresponding to each data line of the electro optic device and loading display data on the scroll bus; and a driving circuit driving the data lines based on the display data loaded in the plurality of data latches; wherein display data of one pixel are read out from a memory cell specified by a word line selected by the display address decoder and a column line selected by the display column address decoder, the data are output to the scroll bus via the read-out bit line coupled to the memory cell, and the data on the scroll bus are loaded in each of the plurality of data latches.

7. **Priem '133** clearly teaches

a plurality of read-out bit lines (column 4, lines 31-32 "data conductors") **each commonly coupled to a memory cell group** (column 4, lines 34-35, "frame buffer memory") **specified by a corresponding column line**

a scroll bus (see column 4, lines 56, "data bus") **coupled to the plurality of read-out bit lines** (see generally last paragraph column 4);

a plurality of data latches (see FIG. 6, "Latch 0" through "Latch 3" and further described in column 2, lines 51-58) **each corresponding to each data line of the electro optic device** (the latches correspond with the data lines of the electro optic device as evidenced in column 2, lines 51-58) **and loading display data on the scroll bus;** (see column 5 lines 39-43) **and**

a driving circuit driving (see column 5, lines 35-44, "circuitry for driving an output display device") **the data lines based on the display data loaded in the plurality of data latches;** (see column 5, lines 33-43)

wherein display data of one pixel are read out from a memory cell (see column 4, lines 65-67 wherein a single 32 bit color pixel is read) **specified by a word line selected by the display address decoder and a column line selected by the display column address decoder, the data are output to the scroll bus via the read-out bit line coupled to the memory cell, and the data on the scroll bus are loaded in each of the plurality of data latches** (same references as above, see the appropriate references).

8. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been motivated to incorporate the method of increasing the rate of scrolling of **Priem '133** in to the display having display memory of **Ikeda** because the **Priem '133** method improves the scrolling speed of a display screen (as is explained in **Priem '133** column 2 lines 41-44).

9. With regard to **claim 2, and as dependent on claim 1, Ikeda** teaches

a shift register (see page 1, paragraph [0004], "shift register" element 205) **outputting a shift output shifted based on a given shift clock** (see page 1, paragraph [0004] "CL2 clock signal for controlling the shift register"; element 215);

wherein each of the plurality of data latches loads display data on the scroll bus based on a shift output of each stage of the shift register. (See page 1, paragraph [0004])

10. With regard to **claim 3 and as dependent on claim 1, Priem '133** teaches

a line latch loading display data that are loaded in the plurality of data latches in one horizontal scan cycle; (see column 8, lines 26-34)

wherein the driving circuit drives the data lines based on display data loaded in the line latches instead of the plurality of data latches. (see column 8, lines 26-34).

11. With regard **to claim 4, as stated above Ikeda in view of Priem '133** clearly discloses **a display driver for driving data lines of an electro optic device based on display data, comprising: a display data random access memory including a plurality of word lines, a**

plurality of column lines, and a plurality of memory cells each storing display data of one pixel; a display address decoder selecting a word line of the display data random access memory based on a display address; a display column address decoder selecting a column line of the display data random access memory based on a display column address; a plurality of read-out bit lines each commonly coupled to a memory cell specified by a column line; (see arguments made above in paragraphs 5-8 of this Office Action).

Furthermore, **Priem '133** clearly discloses

a scroll display data generating circuit (see column 11, lines 23-25 "circuitry for writing the data stored")

including a plurality of data latches that each correspond to each data line of the electro optic device, (see column 11, lines 13-15 "latching circuitry" and as further described in column 2, lines 51-58)

shifting display data of one pixel that are output to each read-out bit line by a shift amount in line with a given scroll amount, (see column 9, lines 57-64 disclosing a method of shifting a pixel; see also column 4, lines 65-67 describing the read and write of a single pixel)

and loading the data in any of the plurality of data latches, so as to generate display data of one horizontal scan line (see paragraph 9, lines 57-64);

and a driving circuit a driving circuit driving (see column 5, lines 35-44, "circuitry for driving an output display device") **driving the data lines based on the**

display data of one horizontal scan line generated by the scroll display data generating circuit. (see column 8, lines 26-34)

12. With regard to **claim 5, and as dependent on claim1, Ikeda** teaches

a plurality of scan lines; (see page 3, paragraph [0026] "plurality of scanning lines")

a plurality of data lines; (see page 3, paragraph [0026] "plurality of data lines")

a plurality of pixels coupled to the plurality of scan lines and the plurality of data lines; (see page 3, paragraph [0026] "pixels being formed at the intersections of the data and scanning lines")

a scan driver scanning the plurality of scan lines; (see page 3, paragraph [0026] "liquid crystal driver... to apply a voltage corresponding to the display data")

13. With regard to **claim 6, and as dependent on claim 1, Ikeda** teaches

a display panel (see page 3, paragraph [0024] "liquid crystal display system") **including**

a plurality of scan lines, (see page 3, paragraph [0026] "plurality of scanning lines")

a plurality of data lines, (see page 3, paragraph [0026] "plurality of data lines") **and**

a plurality of pixels coupled to the plurality of scan lines and the plurality of data lines; (see page 3, paragraph [0026] "pixels being formed at the intersections of the data and scanning lines")

a scan driver scanning the plurality of scan lines; a scan driver scanning the plurality of scan lines. (see page 3, paragraph [0026] "liquid crystal driver... to apply a voltage corresponding to the display data")

14. With regard to **claim 7, and as dependent on claim 5, Ikeda** teaches **a display data generator generating display data to be supplied to the electro optic device.** (see page 22, paragraph [0278], claim 1 "display generating circuit...which generates display data in the form of a plurality of bits for each of a plurality of pixels of a display panel")

15. With regard to **claim 8,** see the reasoning and arguments above in paragraphs 5-8 of this Office Action.

16. With regard to **claim 9, as dependent on claim 8,** see the reasoning and arguments above in paragraph 10 of this Office Action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarvesh J. Nadkarni whose telephone number is 571-270-1541. The examiner can normally be reached on 8:00-5:00 M-Th EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-273-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SN

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER